State of the Art in
MEMORY CLUSTER TESTING
at Board and System Level

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Outline

• Overview of Memory Cluster Test methodologies
• Memory devices with various Test Modes
• Why do we need IEEE P1581?
Types of Memory Cluster Tests

Memory without Test Mode:

Software based functional test:

*functional access by firmware*

- Manual test development;
- What if board/system does not boot up?
Types of Memory Cluster Tests

Memory without Test Mode:

IEEE 1149.1 based cluster test:
access from IEEE 1149.1 in memory host device
  ➔ Long test programs;
  ➔ Timing problems;
Types of Memory Cluster Tests

Memory without Test Mode:

Hardware based BIST:

*functional access by BIST hardware in memory host device*

→ Not widely available;
Types of Memory Cluster Tests

Memory **with** Test Mode:

**Custom test mode:**

- memory pins tested as part of cluster test
  - e.g. NAND Tree, “Boundary Scan” (not compliant to IEEE 1149.1), etc.
  - Not standardized;
Types of Memory Cluster Tests

**Memory with Test Mode:**

**IEEE 1149.1 built in:**

- Memory pins tested in interconnect test
  - No special cluster test required;
  - Four extra pins (IEEE 1149.1 Test Access Port)
Types of Memory Cluster Tests

Memory with Test Mode:

IEEE P1581 built in:
combinatorial test logic in memory

- Automated test development;
- Test access from IEEE 1149.1 devices or through probes;
- Memory core is bypassed, no timing issues;
- Few test vectors;
SDRAM Cluster Test – BScan only

- Functional write and read access to RAM
- Requires control over SDRAM clock
- Example:
  - scan chain of 1900 cells, $TCK = 10$ MHz (typ. less!)
  - Memory cluster test comprises 1840 Shift-DR cycles
  - Total shift time: 350 milliseconds
  - Actual test execution time: $\sim 2$ sec ... 10 sec (or more)
  - File size: $\sim 10$ kByte (binary) ... 100+ kByte (ASCII)
SDRAM Cluster Test – with P1581

- Utilizing combinatorial test logic embedded in RAM
- No timing problems
- Example:
  - *scan chain of 1900 cells, TCK = 10 MHz (typ. less!)*
  - *Memory cluster test comprises 48 Shift-DR cycles*
  - *Total shift time: 9 milliseconds*
  - *Actual test execution time: << 1 sec*
  - *File size: << 1 kByte (binary) ... <10 kByte (ASCII)*
FLASH EEPROM – BScan only

- Check ID codes only
- Read and compare known good data
- Test of FLASH EEPROM based on write and read access:
  - Multiple erase cycles
  - Very time consuming
  - May not be possible
FLASH EEPROM – with P1581

- Combinatorial test logic embedded in FLASH
- No erase required
- First practical test method for FLASH EEPROM

Functional FLASH erase, write, and read access

Functional FLASH access

File size

Time
Conclusion

• State of the art memory cluster test methods have limitations

• IEEE P1581 provides real benefits:
  – *Enabling new test applications*
  – *Improving existing test applications*
  – *Simple implementation, little overhead*
  – *Simple test pattern*
  – *Small test programs (embedded test)*

• Need input from Chip vendors

[http://grouper.ieee.org/groups/1581/](http://grouper.ieee.org/groups/1581/)